REQUESTED AMENDMENTS TO THE CLAIMS

Applicant respectfully requests entry of the following amendments, which include cancellation of claims 1-3, 8, 17, and 26 without prejudice or disclaimer to resubmission in a divisional or continuation application; amendment to claims 4, 8, 18 and 27; and the addition of New claim 28, as reflected in the following Listing of Claims, which is intended to replace all prior versions and Listings of Claims in the application:

1-3. **(Canceled).**

4. **(Currently Amended)** A method comprising:

dividing a high-frequency clock signal into a divided frequency signal in accordance with a data input; and

dividing said divided frequency signal into a further divided frequency signal in accordance with said data input,

~~The method according to claim 1,~~ wherein dividing said high-frequency clock signal comprises:

passing said high-frequency clock signal through a pass gate; and

sampling said high-frequency clock signal.

5. **(Previously Presented)** The method according to claim 4, wherein dividing said high-frequency clock signal further comprises, after said sampling, selectively closing said pass gate in accordance with a count value of said data input.

6. **(Previously Presented)** The method according to claim 5, wherein said selectively closing comprises closing said pass gate if said count value is odd.

7. **(Previously Presented)** The method according to claim 5, wherein said selectively closing comprises using at least one flip-flop.

8. **(Currently Amended)** The method according to claim ~~1~~ 4, wherein dividing said high-frequency clock signal comprises dividing said high-frequency clock signal using a D-type flip-flop that feeds its Q-bar output into its data input.

9-16. **(Canceled).**

17. **(Canceled).**

18. **(Currently Amended)** An apparatus comprising:

a frequency dividing arrangement adapted to divide a high-frequency clock signal into a divided frequency signal in accordance with a data input, and to divide said divided frequency signal into a further divided frequency signal in accordance with said data input,

~~The apparatus of claim 17,~~ wherein said frequency dividing arrangement comprises:

a frequency divider adapted to divide said high-frequency clock signal into said divided frequency signal;

a multi-bit counter adapted to divide said divided frequency signal in accordance with said data input; and

a control configuration to selectively pass said high-frequency clock signal to said frequency divider based on said data input.

19. **(Previously Presented)** The apparatus of claim 18, wherein said frequency divider comprises a dual modulus frequency divider.

20. **(Previously Presented)** The apparatus of claim 18, wherein said frequency divider comprises a D-type flip-flop that feeds its Q-bar output into its data input.

21. **(Previously Presented)** The apparatus of claim 18, wherein said multi-bit counter comprises a 2n-bit counter adapted to receive data inputs DIN<1:(2^n-1)>.

22. **(Previously Presented)** The apparatus of claim 18, wherein said control configuration is adapted to control a count precision of said multi-bit counter.

23. **(Previously Presented)** The apparatus of claim 18, wherein said control configuration comprises a pass gate to be selectively closed based on a count value of said input data.

24. **(Previously Presented)** The apparatus of claim 23, wherein said control configuration comprises at least one flip flop to selectively close said pass gate.

25. **(Previously Presented)** The apparatus of claim 24, wherein said at least one flip flop is able to selectively close said pass gate based on an output of said multi-bit counter.

26. **(Canceled).**

27. **(Currently Amended)** An apparatus comprising:

a frequency dividing arrangement adapted to divide a high-frequency clock signal into a divided frequency signal in accordance with a data input, and to divide said divided frequency signal into a further divided frequency signal in accordance with said data input; and

an integrated circuit associated with said frequency dividing arrangement,

~~The apparatus of claim 26,~~ wherein said frequency dividing arrangement comprises:

a frequency divider adapted to divide said high-frequency clock signal into said divided frequency signal;

a multi-bit counter adapted to divide said divided frequency signal in accordance with said data input; and

a control configuration to selectively pass said high-frequency clock signal to said frequency divider based on said data input.

28. **(New)** The apparatus of claim 27, wherein said control configuration comprises a pass gate to be selectively closed based on a count value of said input data.